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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/460,742	12/14/1999	RAJENDRAN NAIR	884.229US1	2896

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/460,742	NAIR ET AL.	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-6,9,10 and 14-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9,10 and 14-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

This office action is in response to the amendment filed 02/19/02. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 4-6 and 14-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

For claims 4 and 14, the phase "capable of ..." does not positively recite a circuit function and it is not clear whether the claimed function does or does not occurred.

Claims 5-6 and 15-16 are rejected as including the indefiniteness of claim 4.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C.

122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 9-10 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Sin (USP 5130564) (previous cited).

As to claim 9, Sin discloses in figure 5A a circuit comprising a die (semiconductor integrated chip, according to lines 8-10 of column 1) having a high power supply voltage node (N) and a low power supply voltage node (VR); and a transistor (the transistor VTNL in figure 8A forming the variable capacitor VCL in figure 5A) coupled between the high power supply voltage node and the low power supply voltage node and operable for controlling a voltage at the low power supply voltage node.

As to claim 10, figure 8A shows the transistor having a gate coupled to the high power supply voltage node and the source and drain coupled to the low power supply voltage node.

As to claim 14, figure2A-B discloses an electronic device CL permanently coupled between the ground node Vss and the power supply voltage node (node between VPT and VNT), providing an asymmetrical response incremental variations about an operational node voltage VNTL) at the power supply voltage node.

As to claim 15, since electric property of the capacitor CL as shown in figure 2B around point of VTNL is the same as the claimed capacitor transistor whose property is shown in figure 1B of the application and the prior art discloses all the claimed structure, the accompanying characteristics including the damping and amplifying are also inherent.

As to claim 16, the power supply voltage node can be about 1.3 volt at some point during transition of the voltage at the voltage node between VCC and VSS when the driver DRV switches.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Freyman et al. (USP 5828251) in view of Nakai (JP Document-identifier NO. JP 10242414A).

As to claim 4, Freyman et al.'s figure 1 shows a circuit comprising: a voltage node (Vdd); a ground node (Vss); and a transistor (102) including a gate, a drain, and a source, the gate being coupled to the voltage node and the drain and source being coupled to the ground node. Thus, figure 1 show all limitations of the claim except for the transistor comprising a p-type polysilicon. However, Nakai's figure 1 teaches a method of making all gate of NMOS transistor transistors (Qa and Qb) comprises a p-type polisilicon for the purpose of suppress the substrate bias dependency of a the threshold voltage or balancing the circuit in a low-battery-ization process. Therefore, it would have been obvious to one having ordinary skill in the art to make the gate of Freyman et al.'s transistor 102 (and the gate of all n-transistor in the circuit to be comprise p-type polysilicon for the purpose of suppress the substrate bias dependency of a the threshold voltage or balancing the circuit in a low-battery-ization process.

As to claim, it is seen as a design expedience for selecting the value of the operating voltage to be between about .t volt and about 1.5 volt dependent upon particular environment of use to ensure optimum performance.

As to claim 6, Freyman et al.'s figure 1 shows a logic cell (105, 106) coupled to the voltage node and located in close proximity to the transistor.

Response to Arguments

7. Applicant's arguments have been fully considered but they are not persuasive.

In response to the arguments of the rejection of claims 9-10. Applicant states that "in contrast, Sin in figure 5A shows a variable capacitor (VCL) coupled between voltage nodes Vo and VR...Thus, Sin does not teach of the elements recited in claim 9". The Examiner respectfully disagrees. "a high voltage power supply node" and "a low voltage power supply node" are interpreted as two nodes located at difference location. Since, node Vo is supplied with a higher voltage than node VR, node Vo can be considered as a high power supply voltage node and node VR can be consider as a low power supply node.

For the arguments of claims 14-16, Applicant states "Hence, since the CL is not permanently coupled between ground node and Vcc, Sin does not disclose "...an electronic device permanently coupled between the ground node and the power supply voltage node..." as recited in claim 14". The examiner respectfully disagrees. As stated above the "power supply voltage node is interpreted as a node. Since Sin's node between VTP and VTN is supplied by some amount of voltage, that node can be considered a power supply voltage node (for the capacitor). Figure 2A further shows the capacitor is permanently coupled to the output node. Thus, figure 2 meets all limitations of the claims.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
April 6, 2002

Terry D. Cunningham
Primary Examiner